REMARKS

Claims 1, 8, 9, and 11 are pending. Claims 1, 9, and 11 have been amended. Claims 2-7, and 10 have been canceled. No new matter has been introduced. Reexamination and reconsideration of the present application is respectfully requested.

In the December 31, 2007 Office Action, the Examiner rejected claims 1, 8, 9, and 11 under 35 U.S.C. § 103(a) as being unpatentable over Cullen et al., U.S. Patent No. 5,465,304, and further in view of Yasushi, JP 403184476. Applicant respectfully traverses the rejections in view of the claims, as amended.

Independent claim 1, as amended recites:

> A storage device comprising:
> a memory array including a plurality of memory blocks, each of which includes plural lines of cells in correspondence with a data length;
> a first register for storing a first address representing a first cell within a region for storing a specific number of data each having a same value;
> an adder for adding run-length data representing the specific number of the data each having the same value to the first address so as to produce a second address;
> a second register for storing the second address;
> ***a counter for supplying a write address designating a cell of the memory array subjected to a write operation***;
> ***a multiplexer for outputting the write address supplied from the counter to the memory array when performing the write operation and for outputting a read address to the memory array when performing a read operation***; and
> a controller for selecting a certain number of the cells within a line designated by the write address based on the first address and the second address within the memory array to be simultaneously placed in a write-enable state,
> ***wherein, when the region for storing the specific number of data, which are specified by the first address and the second address, lies in two or more lines of the cells, the counter increases the write address from a first write address to a second write address during execution of the write operation for writing the data into the region, the controller changes the cells, which are simultaneously placed in the write-enable state, from a first number of cells designated by the first write address within a first line to a second number of cells designated by the second write address within a second line.***

The Cullen reference does not disclose, teach, or suggest the storage device specified in

independent claim 1, as amended. Unlike the apparatus specified in claim 1, as amended, Cullen does not teach a device which includes "***storing the specific number of data, which are specified by the first address and the second address, lies in two or more lines of the cells, the counter increases the write address from a first write address to a second write address during execution of the write operation for writing the data into the region, the controller changes the cells, which are simultaneously placed in the write-enable state, from a first number of cells designated by the first write address within a first line to a second number of cells designated by the second write address within a second line.***"

Moreover, Cullen fails to disclose, teach, or suggest "***a counter for supplying a write address designating a cell of the memory array subjected to a write operation***" or "***a multiplexer for outputting the write address supplied from the counter to the memory array when performing the write operation and for outputting a read address to the memory array when performing a read operation***" as specified in claim 1, as amended.

The Cullen reference teaches a character recognition system that segments a scanned document image into areas containing text and non-text. In the scan line compression shown in FIG. 3, four horizontal scan lines 300-303 are collectively compressed into a single scan line; then, after completion of the image compression, the run length relative to the consecutive black blocks is extracted. FIG. 4 shows the scan line and run length of pixels, wherein, within the consecutive black pixels 402, the pixel 403 designates a start point of the run length, and the pixel 404 designates an end point of the run length. The pixel 403 corresponds to the address 312, and the pixel 404 corresponds to the address 440. *(Cullen, Col. 9, line 58 to Col. 10, line 19)* When the run length is extracted based on the compressed scan line, a rectangular region representing the features of a document is formed. The rectangular region includes consecutive

black pixels in a two-dimensional manner.

The Cullen reference may describe the creation of run lengths (i.e., the method for compressing images); however, it fails to teach, disclose, or suggest the mechanism of the subject invention, in which data already subjected to run-length coding is decoded, so that the decoded data is written into a line of cells designated by the write address supplied from the counter within the memory array, wherein when the region for storing the specific number of data lies in two or more lines of cells, the counter increases the write address so as to perform the write operation on each of the lines designated by the increased write address. Accordingly, Applicant respectfully submits that independent claim 1, as amended distinguishes over the Cullen reference.

The Yasushi reference teaches an image processing device for drawing image data of 32-bit horizontal lines including bits "0" (white) and "1" (black). FIG. 1 is a functional block diagram of this image processing device. In FIG. 1, the reference numeral 2 designates registers, including 16-bit registers 3 and 4, which are assigned with consecutive addresses 0 to 31. A selector, designated by 8, selects image data of a single horizontal line that is written into the registers 2, wherein the registers 3 and 4 are designated in order under the instruction of a bus master so as to sequentially output data of the registers 3 and 4 onto the data bus 9. In this embodiment, image data containing seventeen bits of "0" (white) and fifteen bits of "1" (black) is written into a single horizontal line shown in FIG. 3.

After initialization of all the bits of the registers 2 is completed, the image data consisting of seventeen bits of "0" is written into the write end pointer 7. Correspondingly, an end pointer is calculated based on the start pointer and image data, in which (end pointer) = (start pointer) + (length of image data) – 1 = 16, which results in the end pointer being rewritten as "16."

Furthermore, the write signal generation circuit 5 makes a write signal regarding seventeen bits of "0" (white) active, so that a binary signal (i.e. "0") input to the write end pointer 7 is written into the registers 2 ranging from bit 0 to bit 16 simultaneously. Then, a start pointer set signal is output to the write start pointer 5, which then performs the calculation of (end pointer) + 1, which outputs the resulting calculation as the start pointer. The new start pointer is set to the write start pointer 5, so that the bus master outputs the next image data of fifteen bits of "1" (black) to the write end pointer 7, whereby "1" is written into the registers 2 ranging from bit 17 to bit 32. The selector 8 sequentially selects the registers 3 and 4 so that 16-bit data are each output to the bus master.

The Yasushi reference may teach the process for writing image data having the same value into the registers (including the 16-bit registers). However, Yasushi fails to disclose, teach, or suggest the mechanism of the subject invention, in which data already subjected to run-length coding is decoded, so that the decoded data is written into a line of cells designated by the write address supplied from the counter within the memory array, wherein when the region for storing the specific number of data lies in two or more lines of cells, the counter increases the write address so as to perform the write operation on each of the lines designated by the increased write address. Accordingly, Applicant respectfully submits that independent claim 1, as amended distinguishes over the Yasushi reference..

Accordingly, both the Cullen and Yasushi references do not disclose, teach, or suggest the technical features of the subject invention. Therefore, Applicant respectfully submits that independent claim 1, as amended distinguishes over Cullen in combination with Yasushi.

Independent claims 9 and 11 recite limitations similar to those in independent claim 1, as amended. Accordingly, Applicant respectfully submits that independent claims 9 and 11

the technical features of the subject invention. Therefore, Applicant respectfully submits that independent claim 1, as amended distinguishes over Cullen in combination with Yasushi.

Independent claims 9 and 11 recite limitations similar to those in independent claim 1, as amended. Accordingly, Applicant respectfully submits that independent claims 9 and 11 distinguish over Cullen in combination with Yasushi for reasons similar to those set forth above with respect to independent claim 1, as amended.

Claim 8 depends from independent claim 1, as amended. Accordingly, Applicant respectfully submits that claim 8 distinguishes over Cullen in combination with Yasushi for the same reasons set forth above with respect to independent claim 1.

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Applicant believes that the claims are in condition for allowance. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference call would advance prosecution of the application.

Respectfully submitted,

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By: _____

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